L Number	Hits	Search Text	DB	Time stamp
1	15385	(detect$3 or monitor$3 or decode$1 or decoding) near3 data near2 process$3	USPAT; US-PGPUB	2002/09/15 16:20
4	95593	(power or energy) near (manage$4 or save$1 or saving$1 or reduce$1 or reducing or reduction)	USPAT; US-PGPUB	2002/09/15 16:21
7	49	((detect$3 or monitor$3 or decode$1 or decoding) near3 data near2 process$3) same ((power or energy) near (manage$4 or save$1 or saving$1 or reduce$1 or reducing or reduction))	USPAT; US-PGPUB	2002/09/15 15:32
10	7980	(detect$3 or monitor$3 or decode$1 or decoding) near3 data near2 process$3	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 16:21
15	115693	(power or energy) near (manage$4 or save$1 or saving$1 or reduce$1 or reducing or reduction)	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 16:21
20	20	((detect$3 or monitor$3 or decode$1 or decoding) near3 data near2 process$3) same ((power or energy) near (manage$4 or save$1 or saving$1 or reduce$1 or reducing or reduction))	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 16:21
-	2330	mode adj2 table$1	USPAT; US-PGPUB	2002/09/15 11:37
-	2	(power adj2 save) with (mode adj2 table$1)	USPAT; US-PGPUB	2002/09/15 11:38
-	460	mode adj2 table$1	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:04
-	1	(power adj2 save) with (mode adj2 table$1)	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:23
-	182720	data near2 process$3	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:23
-	27	(power adj2 save) with (data near2 process$3)	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:23
-	14291	function$2 adj unit$1	USPAT; US-PGPUB	2002/09/15 11:38
-	0	(power adj2 save) with (function$2 adj unit$1)	USPAT; US-PGPUB	2002/09/15 11:38
-	1	(power adj2 save) same (function$2 adj unit$1)	USPAT; US-PGPUB	2002/09/15 11:39
-	112	((power or turn$3) adj2 off) same (function$2 adj unit$1)	USPAT; US-PGPUB	2002/09/15 11:41
-	11521	713/$.ccls.	USPAT; US-PGPUB	2002/09/15 11:41
-	21	713/$.ccls. and (((power or turn$3) adj2 off) same (function$2 adj unit$1))	USPAT; US-PGPUB	2002/09/15 12:00
-	94	mittal$.in.	USPAT; US-PGPUB	2002/09/15 12:03
-	1	mittal$.in. and 713/$.ccls.	USPAT; US-PGPUB	2002/09/15 12:01
-	29	mital$.in.	USPAT; US-PGPUB	2002/09/15 12:03
-	0	713/$.ccls. and mital$.in.	USPAT; US-PGPUB	2002/09/15 15:26

09/285,879

US-PAT-NO: 6219796
DOCUMENT-IDENTIFIER: US 6219796 B1

TITLE: Power reduction for processors by software control of functional units

DATE-ISSUED: April 17, 2001

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
Bartley; David Harold	Dallas	TX	N/A	N/A

US-CL-CURRENT: **713/320**; 712/214 ; **713/324**

ABSTRACT:

   A method of optimizing a computer program for reduced power consumption by a
processor (10) having functional units (11d, 11e) that are independently
controllable by instructions. The processor's instruction set (FIG. 4) has
instructions that may be directed to a particular functional unit (11d, 11e) so
as to place that functional unit in a power-down state while not being used
during a program segment.

9 Claims, 8 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

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Detailed Description Text - DETX:

As further illustrated in FIG. 6, one or more additional instruction types may
be added to place **functional units** into intermediate power-down levels. In a
"less ready" state, a **functional unit** would consume less or no power. In a
"more ready" state, it would consume more power but could be more quickly be
made ready for use. For example, in addition to the SLEEP instruction type,
the instruction set of processor 10 has a REST instruction type. An example of
implementation of an intermediate power-down instruction is one that **turns off**
all circuitry of a **functional unit** other than memory that is private to that
functional unit.

Detailed Description Text - DETX:

FIG. 7 illustrates the basic steps of an optimization process in accordance
with the invention. As illustrated, for each **functional unit,** the program code
is scanned to identify segments where the **functional unit** is not used. The
identification of an "inactive segment" made in terms of efficiency. Various
power modeling techniques can be used to determine the length of time during
which it is more efficient to **turn a component off** (or partially off) then on
again versus leaving it on. The resulting "power down threshold" might be
different for different **functional units** and for different power-down levels.

Current US Original Classification - CCOR:

713/320

Current US Cross Reference Classification - CCXR:

713/324

US-PAT-NO: 5832280
DOCUMENT-IDENTIFIER: US 5832280 A

TITLE: Method and system in a data processing system for interfacing an
operating system with a power management controller.

DATE-ISSUED: November 3, 1998

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
Swanberg; Randal Craig	Round Rock	TX	N/A	N/A

US-CL-CURRENT: **713/300**; 710/14 ; 710/8 ; 710/9 ; **713/323**

ABSTRACT:

    In a data processing system having an operating system and a power
management controller coupled to one or more power-managed devices, each of the
power-managed devices is assigned a device identifier. An architected
power-managed device select register and an architected power mode select
register are provided within the data processing system. To modify a power
mode of a power-managed device, the operating system writes a selected one of
the device identifiers to the architected power-managed device select register
for selecting an identified one of the power-managed devices. Thereafter, the
operating system writes a power mode identifier to the architect power mode
select register for selecting one of a plurality of power modes within the
selected power-managed device. The device identifier and the power mode
identifier are translated into control signals for the power management
controller within the data processing system. Such control signals are then
transmitted to the power management controller and the identified power-managed
device is operated in the selected power mode, wherein the operating system
controls the power modes of power-managed devices without programming a
particular implementation of power management control in the operating system.

10 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

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Brief Summary Text - BSTX:

The control of power consumption within a data processing system has become
increasingly important, particularly since portable data processing systems
that use a self-contained power source have become popular. Such a
self-contained power source is typically a battery. In order to maximize the
amount of data processing that may be done using the power stored in a
reasonably sized battery, various **functional units** within the data processing
system may be disconnected from the battery power source, or operated in a
lower power consuming mode, until the full function of a particular unit is
needed. Examples of such **functional units** include hard disk drives, floppy
disk drives, modems, display devices, CD-ROM drives, and the like. Each of
these devices may be designed to operate in a plurality of power modes. For
example, a simple set of power modes may include a "power on" mode and a "**power
off**" mode. Other power modes may include a low power mode that retains the

state of the **functional unit** in memory, a low power mode that retains a partial
state of the **functional unit,** and a low power mode that does not retain any
state of the **functional unit**.

Current US Original Classification - CCOR:

713/300

Current US Cross Reference Classification - CCXR:

713/323

US-PAT-NO: 5815724
DOCUMENT-IDENTIFIER: US 5815724 A

TITLE: Method and apparatus for controlling power consumption in a
microprocessor

DATE-ISSUED: September 29, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mates; John William Benson	Portland	OR	N/A	N/A

US-CL-CURRENT: **713/322**; 712/242 ; 712/243 ; **713/321** ; **713/323** ; **713/601**

ABSTRACT:

    A system for controlling power consumption in a microprocessor. The
microprocessor fetches an instruction from memory. The instruction is decoded,
producing an operation flow of at least one operation. Then, power
micro-operations are introduced into the operation flow. These power
micro-operations provide power consumption control functions for those
functional units which are required to execute the various operations which
have been decoded from the fetched instruction. The operations and power
micro-operations are then scheduled for dispatch to the appropriate execution
units. The scheduling is based on the availability of the appropriate
execution units and the validity of operation data. The operations and power
micro-operations are dispatched to the appropriate execution units, where the
operations and power micro-operations are executed. The execution results are
subsequently committed to the processor state in the original program order.

24 Claims, 4 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 4

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Detailed Description Text - DETX:

Although the following embodiment is described using a floating point addition
instruction and a floating point execution unit, the present invention may be
practiced with other types of instructions and **functional units** as well. For
example, the present invention may be practiced to enable a **functional unit**
that accesses memory when an instruction is decoded that requires a memory
access. In this manner, a microprocessor implemented in accordance with the
present invention can efficiently control power consumption, since only the
required **functional units** are enabled at a given time. Further, the present
invention may be practiced to offer other types of power consumption control to
the **functional units other than turning the units on or off**.

Detailed Description Text - DETX:

FIG. 1 depicts one embodiment of a method for fetching, decoding, executing,
and writing results in accordance with the present invention. The method of

FIG. 1 includes the insertion of power micro-operations, or P.mu.Ops, into the operation flow. The P.mu.Ops provide system-transparent power management control functions which enable and disable various **functional units** depending on the requirements of the operation flow. Referring again to FIG. 1, in the Fetch Instruction step 110, a macroinstruction is fetched from memory . In this example, the macroinstruction fetched is FADD m32 real, which adds a 32 bit floating point number stored in memory to a 32 bit floating point number stored on top of the stack, and stores the results on top of the stack. Once the macroinstruction is fetched from memory, it is decoded at the Decode Instruction/Insert P.mu.Ops step 120. At this step, the FADD m32 real macroinstruction is broken down into a number of micro-operations (.mu.Ops). In this example, the .mu.Ops specify that the contents of the stack be placed in a floating point register FPR1, that the contents of memory location m32 real be moved to another floating point register FPR2, that the contents of FPR1 and FPR2 be added, and that the results of the addition are stored on top of the stack. In addition, two P.mu.Ops are inserted into the operation flow. To determine which P.mu.Ops to insert, at the Decode Instruction/Insert P.mu.Ops step 120, the macroinstruction is examined to determine which **functional units** are required in order to execute the decoded macroinstruction. For example, the P.mu.Ops specify that the Floating Point Execution Unit (FEU) is turned on before the floating point addition occurs and **turned off** again after the floating point addition has completed.

Detailed Description Text - DETX:

In order to schedule the .mu.Ops and P.mu.Ops for the execution units in the Execution Cluster 340, the RS 362 ascertains which .mu.Ops and P.mu.Ops are data ready by evaluating a corresponding data valid bit for each source data. The RS 362 then determines availability of execution units for data ready .mu.Ops and P.mu.Ops, and schedules the .mu.Ops and P.mu.Ops based on a priority pointer. The P.mu.Ops are scheduled in a way that ensures that the various **functional units** required to execute the other .mu.Ops stored in the RS 362 are enabled during the required periods of time. The RS 362 may also be implemented to look for situations where a particular **functional unit** is scheduled to be **turned on and off** repeatedly, for example where a series of floating point operations are scheduled to be executed in the Floating Point Execution Unit (FEU) 343. In such a case, the RS 362 would not schedule the P.mu.Ops to **turn on and off** the FEU for each floating point operation, but would rather schedule the P.mu.Ops so that the FEU 343 was turned on before executing the first floating point operation in the series and then **turned off** after the last floating point operation in the series was executed. Also, the P.mu.Ops are scheduled to be executed in parallel with other .mu.Ops or P.mu.Ops whenever possible, thus ensuring that any degradation in the otherwise available performance will be minimized. For the scheduled .mu.Ops and P.mu.Ops, the RS 362 dispatches the .mu.Ops and P.mu.Ops and associated source data to the appropriate execution unit.

Current US Original Classification - CCOR:

713/322

Current US Cross Reference Classification - CCXR:

713/321

Current US Cross Reference Classification - CCXR:

713/323

Current US Cross Reference Classification - CCXR:

713/601

US-PAT-NO: 5787297
DOCUMENT-IDENTIFIER: US 5787297 A

TITLE: Selective power-down for high performance CPU/system

DATE-ISSUED: July 28, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lin; Chong Ming	Sunnyvale	CA	N/A	N/A

US-CL-CURRENT: **713/322**; **713/310** ; **713/321** ; **713/324**

ABSTRACT:

   A microelectronic device according to the present invention is made up of
two or more **functional units,** which are all disposed on a single chip, or die.
The present invention works on the strategy that all of the **functional units** on
the die are not, and do not need to be operational at a given time in the
execution of a computer program that is controlling the microelectronic device.
The present invention on a very rapid basis (typically a half clock cycle),
therefore, **turns on and off the functional units** of the microelectronic device
in accordance with the requirements of the program being executed. This power
down can be achieved by one of three techniques; **turning off** clock inputs to
the **functional units,** interrupting the supply of power to the **functional units,**
or deactivating input signals to the **functional units**. The operation of the
present invention results in a very significant reduction in power consumption
and corresponding heat dissipation by the microelectronic device as compared to
the conventional approach of keeping all **functional units** operational all of
the time.

12 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

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Abstract Text - ABTX:

Brief Summary Text - BSTX:

A microelectronic device according to the present invention is made up of two or more **functional units,** which are all disposed on a single chip, or die. The present invention works on the strategy that all of the **functional units** on the die are not, and do not need to be operational at a given time in the execution of a computer program that is controlling the microelectronic device. The present invention on a very rapid basis (typically a half clock cycle), therefore, **turns on and off the functional units** of the microelectronic device in accordance with the requirements of the program being executed. The operation of the present invention results in a very significant reduction in power consumption and corresponding heat dissipation by the microelectronic device as compared to the conventional approach of keeping all **functional units** operational all of the time.

Brief Summary Text - BSTX:

If the **functional units** are divided into still smaller blocks, then a higher percentage of units/blocks can be **turned off,** given that the necessary control logic necessary to perform the switching does not add too much overhead.

Brief Summary Text - BSTX:

The present invention utilizes several approaches for determining when to **turn on and off the functional units** of the microelectronic device. One approach utilizes the compiler which compiles the source code of the computer program into machine code used to control the operation of the microelectronic device. A logic unit evaluates (e.g., decodes or monitors) the machine code during execution, and based on utilization information provided by the compiler, determines at each step in the execution of the computer program which **functional units** are needed for execution, and therefore should be **turned on or off**. For example, a graphics unit may not need to run when non-graphic operations are executing. Similarly, floating point units (FPU) only run 20-30% of the time in a conventional workstation, thus, it does not need to be on during idle periods. Cache memory units also lend themselves to control based on the present invention.

Brief Summary Text - BSTX:

Another approach used by the present invention for determining when to **turn on and off the functional units** is that performed using a logic unit on the die that evaluates (monitors) the execution and operation of the **functional units**. This monitoring function produces indications of upcoming operation (including execution and latency to complete the issued instruction) that can be used for controlling the **turn on/turn off** operation of the present invention. In a compact on-chip low cost FPU, for example, not all the units can be used at the same time or a collision can result. When an FALU operation is being executed, the multiplier or divider may not be pemitted to run. Power can therefore be shut off to these units.

Brief Summary Text - BSTX:

Any suitable preselected amount of time can be used by the present invention for **turning on and for tuning off the functional units** in accordance with the requirements of the computer program that is being executed. The **turn on/turn off** can be as fast as a half-clock cycle, if desired, so as to produce maximum power dissipation saving and power consumption reduction. Other clock cycle

periods for **turn on and for turn off** can be used. Another method is **turning on and off** power line(s) to a selected block or blocks.

Brief Summary Text - BSTX:

The present invention contemplates any appropriate electronic approach for **turning on and off a functional unit**. In complementary metal oxide semiconductor (CMOS) circuits, a preferred approach is either (1) to stop the clock signal to the **functional unit that .is being turned off,** or (2) to stop the inputs of the **functional unit being turned off** from changing. Either approach produces the desired result of **turning off the functional unit The functional unit** can be subsequently turned on by the opposite approach that is used for **turning it off**.

Drawing Description Text - DRTX:

FIG. 4 is a block diagram of an embodiment of the present invention for **turning on and off the functional units** using the system clock signal with gated control signal.

Drawing Description Text - DRTX:

FIG. 5 is a block diagram of an embodiment of the present invention for **turning on and off the functional units** by controlling the state of the inputs to the **functional units**.

Detailed Description Text - DETX:

The present invention is a system and method for selectively controlling the power provided to each of the **functional units** of a microelectronic device so that the **functional units** can be **turned on and off** as needed by the execution of the computer program that is controlling the microelectronic device. The dynamic **turning on and off of the functional units** in accordance with the requirements of the program step(s) being executed causes a significant reduction in power (e.g., 10-30%) consumed by the **functional units,** which results in significant reduction in the heat dissipation requirements and a significant reduction in the power requirements of the microelectronic device. The present invention results in significant reduction in heat dissipation requirements and in power requirements for the microelectronic device, which means that heat sink requirements are reduced and battery discharge cycle length is extended, both of which are very desirable results. In addition, power bus line widths can be reduced. This leads to substantial area saving for VLSI chips.

Detailed Description Text - DETX:

As shown in FIG. 1, a logic unit 116 is part of microelectronic device 100. Logic unit 116, as discussed in greater detail below, operates with system clock 104 so as to determine when to **turn on and off,** and to actually **turn on and off** the supply of clock signals to the **functional units** in accordance with one embodiment of the present invention.

Detailed Description Text - DETX:

The fourth and final step or block of the present invention is represented by a reference numeral 208. In this fourth step, switching ability is no longer provided to the **functional unit** after a preselected clock cycle period (called

clock power down CKPWRDN) after the **functional unit** has completed the required task of executing the machine code instruction of the computer program. In other words, the **functional unit is turned off** (de-activated) after it has executed the required task. In this way, the **functional unit** is not kept on or active after it is no longer needed. A typical value for CKPWRDN is a single half-clock cycle. This activate/de-activate embodiment is appropriate for **functional units** requiring memory, state saving, or the like. Other techniques are well within the scope of the present invention.

Detailed Description Text - DETX:

Coupling/decoupling of a power supply bus is also envisioned. The addition of a power switch(es) connected between V.sub.DD and each **functional unit,** can be used to **turn on and off** the supply of power to the **functional units** by controlling the power switch (e.g., FET) using the above CKPWRON control signal, or the like. In this power-down case, some DC power will be consumed through the power switch, but with the **functional unit**(s) disconnected, overall conservation will result.

Detailed Description Text - DETX:

Referring now to FIG. 4, one representative approach for controlling the state of a **functional unit** in accordance with the present invention is shown. This approach controls providing system clock signal 302 to the **functional unit** in question. The **functional unit** only consumes power when the present invention provides system clock signal 302. Referring now to FIG. 4, logical unit 116 of the present invention evaluates (by decoding for example) issuance of machine code instructions via a path 402 in accordance with any suitable approach, discussed below. Intelligence provided by path 402 allows logic unit 116 to know when to **turn on and off various functional units** in accordance with the present invention.

Detailed Description Text - DETX:

In operation, logic unit 116 provides system clock signal 302 on the appropriate clock input line for the **functional unit** that is being turned on. When that **functional unit is to be turned off,** logical unit 116 no longer provides system clock 302. Since the **functional unit** cannot change state without provision of the clock signal, no power is consumed by **functional units** not receiving clock signal 302. This is how a **functional unit is turned on or off** by turning clock signal 302 on or off.

Detailed Description Text - DETX:

An alternate approach for **turning on and off the functional units** is shown in FIG. 5. Referring now to FIG. 5, this embodiment **turns on and off functional units** 406, 410, 414, and 418 by controlling the state change of the inputs for these **functional units**. By not allowing the inputs of **functional units** that are off to change state, this approach effectively **turns off such functional units**. Only the inputs of **functional units** that are on are allowed to change state.

Detailed Description Text - DETX:

The present invention contemplates other approaches for **turning on and off functional units** by the logic unit 116. The embodiments of FIGS. 4 and 5 are merely for purposes of illustration.

Detailed Description Text - DETX:

The present invention can utilize several approaches for obtaining the
monitoring information on line 402 used by logic unit 116 to determine when to
turn on and off each of the functional units during the execution of the
machine code instructions.

Current US Original Classification - CCOR:

713/322

Current US Cross Reference Classification - CCXR:

713/310

Current US Cross Reference Classification - CCXR:

713/321

Current US Cross Reference Classification - CCXR:

713/324

US-PAT-NO: 5537650
DOCUMENT-IDENTIFIER: US 5537650 A

TITLE: Method and apparatus for power management in video subsystems

DATE-ISSUED: July 16, 1996

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
West; Roderick M. P.	Colchester	VT	N/A	N/A
Rickard; Kathryn E.	Romsey	N/A	N/A	GB
Grupp; Richard J.	Milton	VT	N/A	N/A

US-CL-CURRENT: **713/324**

ABSTRACT:

   Video subsystem power savings are achieved by shutting off power to unused
subcircuits during blanking. Digital circuitry within the video subsystem not
used during blanking is shut-down by **turning off** the clock thereto. Analog
circuitry within a digital to analog converter is shut-down by **turning off** the
constant current reference thereto. A **functional unit** containing digital
circuitry within a serializer palette digital to analog converter (SPDAC) is
shut-down by **turning off** the clock thereto during system operation in a mode
where the **functional unit** is not utilized. A computer system having a
monochrome display saves **power by shutting off** DAC digital circuitry clocks and
DAC analog circuitry constant current references of all DACs but one. A
portable computer with a liquid crystal display (LCD), a SPDAC for driving an
external display and a LCD controller, saves power by shutting down video
subsystem **functional units** and analog DAC circuitry not used for driving the
LCD. Digital circuitry within the LCD controller is shut-down when an external
display is being driven. In a portable computer operating in a SUSPEND state,
video subsystem **functional units** are shut-down.

17 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX:

subsystem **functional units** and analog DAC circuitry not used for driving the LCD. Digital circuitry within the LCD controller is shut-down when an external display is being driven. In a portable computer operating in a SUSPEND state, video subsystem **functional units** are shut-down.

Detailed Description Text - DETX:

Subcircuits containing CMOS digital circuitry (i.e., **functional units**) can be **turned off by turning off** the clock signal that the digital circuitry requires to operate. Likewise, the digital circuitry can be turned back on by turning back on the clock signal. The digital to analog converters in a video subsystem that present analog display data to the display often have a constant current reference associated with the analog circuitry within them. With the constant current reference **turned off,** the DAC analog circuitry consumes almost no power. Thus, in the context of DAC analog circuitry in the first embodiment, **turning off** power to the analog circuitry can be accomplished by **turning off** the constant current reference associated therewith. Power to the DAC analog circuitry can be restored by turning the constant current reference back on. A specific example of circuitry to implement the first embodiment is shown in FIGS. 5 and 6, and will subsequently be described in greater detail.

Detailed Description Text - DETX:

In a second embodiment of the present invention, a method for reducing power dissipation in a video subsystem based on operating mode is provided. The clock signal to a given **functional unit** can be shut off independent of other **functional unit** clock signals. In the simplest form, the video subsystem, according to the present invention, has two **functional units** and is capable of operating in two different operating modes. In the first operating mode, the first **functional unit** is utilized and the second is not. In the second mode, the second **functional unit** is utilized and the first is not. Thus, the current operating mode must be monitored for. In response to operation in the first operating mode, the clock to the first **functional unit** is turned on and the clock to the second **functional unit is turned off**. Likewise, in response to operation in the second operating mode, the clock to the second **functional unit** is turned on and the clock to the first **functional unit is turned off**.

Detailed Description Text - DETX:

SPDAC 35 comprises several subcircuits implemented in digital circuitry. Subcircuits which include digital circuitry will be referred to as "**functional units.**" **The functional units** of SPDAC 35 include: serializer 42; PSRAM 50; DIRCOL 48; text/attribute logic (TATR) 44; and sprite logic (SPRLO) 52. SPDAC 35, and most SPDACs, operate in several different modes. For example, SPDAC 35 has, among others, a text mode and two graphics modes. In any given mode, not all the **functional units** are utilized. Thus, during a given mode, a **functional unit** not used can be shut-down by **turning off** its clock, yielding a significant digital power savings.

Detailed Description Text - DETX:

The LCDC 96, palette update control 78, PSRAM 76 and MISR 92 are **functional units**. Although DACs 80, 82 and 84 are **functional units,** they also contain analog circuitry having an associated constant current reference thereto. As in the first embodiment, **functional units** can be shut-down by **turning off** their clock and analog circuitry having an associated constant current reference can be shut off by shutting off the constant current reference. Thus, when the display signal indicates that an external CRT display is sought to be driven, LCDC 96 may be shut off. When the display signal indicates that LCD 98 is

sought to be driven, all **functional units** and analog circuitry having a constant current reference thereto used to drive an external CRT display may be shut-down. In the context of FIG. 4, **functional units** including DACs 80, 82 and 84, PSRAM 76, palette update control 78 and MISR 92 are shut-down. In addition, analog circuitry within DACs 80, 82 and 84 are shut-down as well. It will be understood that circuitry similar to that shown in FIGS. 5 and 6 could be used to implement the fourth embodiment.

Detailed Description Text - DETX:

In a fifth embodiment of the present invention, a SUSPEND signal is generated indicating that a SUSPEND state is about to be entered. The SUSPEND signal is monitored for, and in response thereto all **functional units** within the video subsystem are **turned off**. When there is input to the computer, power to the **functional units** within the video subsystem is restored. As in prior embodiments, the **functional units are turned off by turning off** the clock thereto and turned on by turning on the clock.

Detailed Description Text - DETX:

Although not typically part of a SPDAC chip, the so-called cathode ray tube controller (CRTC) in a portable computer system is part of the video subsystem 24 generally found in controller 28, and may benefit from SPDAC digital power management. Often, SPDAC chips are the clock source to the CRTC **functional unit,** since the CRTC clock typically has a period that is a multiple of the pixel clock period. When a portable computer enters a SUSPEND state, there is no reason to operate any **functional unit** involved in video display. Thus, the CRTC can be shut-down when the SPDAC clock sources are **turned off** during the SUSPEND state.

Claims Text - CLTX:

2. The method of claim 1, wherein said plurality of subcircuits includes a **functional unit** comprising digital circuitry operating according to a clock signal, and said step of **turning off** power comprises preventing said clock signal from reaching said digital circuitry.

Claims Text - CLTX:

10. The apparatus of claim 9, wherein said plurality of subcircuits includes one or more **functional units** including digital circuitry operating according to a clock signal, said means for **turning off** power comprises means for preventing said clock signal from reaching said digital circuitry and said means for restoring power comprises means for allowing said clock signal to reach said digital circuitry.

Current US Original Classification - CCOR:

713/324

L Number	Hits	Search Text	DB	Time stamp
1	2330	mode adj2 table$1	USPAT; US-PGPUB	2002/09/15 11:37
4	2	(power adj2 save) with (mode adj2 table$1)	USPAT; US-PGPUB	2002/09/15 11:38
7	460	mode adj2 table$1	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:04
12	1	(power adj2 save) with (mode adj2 table$1)	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:23
17	182720	data near2 process$3	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:23
22	27	(power adj2 save) with (data near2 process$3)	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:23
27	14291	function$2 adj unit$1	USPAT; US-PGPUB	2002/09/15 11:38
30	0	(power adj2 save) with (function$2 adj unit$1)	USPAT; US-PGPUB	2002/09/15 11:38
33	1	(power adj2 save) same (function$2 adj unit$1)	USPAT; US-PGPUB	2002/09/15 11:39
36	112	((power or turn$3) adj2 off) same (function$2 adj unit$1)	USPAT; US-PGPUB	2002/09/15 11:41
39	11521	713/$.ccls.	USPAT; US-PGPUB	2002/09/15 11:41
42	21	713/$.ccls. and (((power or turn$3) adj2 off) same (function$2 adj unit$1))	USPAT; US-PGPUB	2002/09/15 12:00
45	94	mittal$.in.	USPAT; US-PGPUB	2002/09/15 12:03
48	1	mittal$.in. and 713/$.ccls.	USPAT; US-PGPUB	2002/09/15 12:01
51	29	mital$.in.	USPAT; US-PGPUB	2002/09/15 12:03
54	0	713/$.ccls. and mital$.in.	USPAT; US-PGPUB	2002/09/15 12:03

US-PAT-NO: 6105142
DOCUMENT-IDENTIFIER: US 6105142 A

TITLE: Intelligent power management interface for computer system hardware

DATE-ISSUED: August 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Goff; Lonnie C.	Tempe	AZ	N/A	N/A
Evoy; David R.	Tempe	AZ	N/A	N/A
Story; Franklyn	Candler	AZ	N/A	N/A
Sullivan; Mark	Tempe	AZ	N/A	N/A

US-CL-CURRENT: 713/324; 713/320 ; 713/322 ; 713/323

ABSTRACT:

A method and apparatus for managing power consumption in a computer system wherein the method and apparatus is compliant with the proposed Advanced Configuration and Power Interface (ACPI) specification. In one embodiment, a power management processor is sandwiched between platform hardware and the ACPI register layer. The processor processes all operating power management commands and requests while remaining transparent to the user and the operating system. In so doing, routine power management functions, so classified by the operating system, are implemented by the operating system. Sophisticated power management features, on the other hand, are implemented by the present invention independent from operating system control. Accordingly, in the present invention, the operating system need not suspend processing of other threads to process sophisticated power management procedures.

10 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

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Detailed Description Text - DETX:

Power management processor 314 monitors all commands or data directed to registers 116 from ACPI driver 122, ACPI BIOS 118, or ACPI tables 120. Power management processor 314 then analyzes the commands and data and determines the appropriate power states for platform hardware 124. Power management processor 314 of the present invention directly interfaces with various controls, controllers and sensors and status indicators for the power plane controls, clock division control, temperature sensor, voltage control, frequency control, battery controller, real time clock, power button, USB, embedded controllers, dock status, PLL controller and lid status indicators (not shown).

US-PAT-NO: 5623684
DOCUMENT-IDENTIFIER: US 5623684 A

TITLE: Application specific processor architecture comprising pre-designed reconfigurable application elements interconnected via a bus with high-level statements controlling configuration and data routing

DATE-ISSUED: April 22, 1997

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
El-Ghoroury; Hussein S.	Carlsbad	CA	N/A	N/A
McNeill; Dale A.	Encinitas	CA	N/A	N/A
Krause; Charles A.	Carlsbad	CA	N/A	N/A

US-CL-CURRENT: 712/37; 712/1

ABSTRACT:

    The architecture and design method of an application specific processor ("ASP") is disclosed. The ASP is designed by integrating selected pre-designed application elements contained in a library. These selected application elements can communicate with each other via a bus. Post-synthesis tailoring of the synthesized ASP is accomplished by using an instruction program which sequences the invocation of each application element and provides reconfiguration and data input/output routing commands thereto. A power management design is incorporated within the application elements allowing the majority of the application elements to be turned on only during periods of invocation.

18 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

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Detailed Description Text - DETX:

The demodulated data is further processed by autonomous application syntax. These application syntax are activated at the downlink frame clock epoch, process the data, and then shutdown until the next downlink frame clock epoch. This results in substantial **power savings** during operation. In modem 400, each autonomous application syntax maintains its input and output in shared memory syntax 416. FIG. 6 shows the data flow among the centralized controlled demodulation cluster 430 and the distributed controlled data processing syntax. Signals received by modem 400 on line 432 are demodulated by demodulation cluster 430. The demodulated data is placed in a demodulation data segment 460 of shared memory syntax 416 via command/data bus 498, which consists of a portion of command/data/timing bus 499. This demodulated data is subsequently processed by deinterleaver 409. The result is stored in a deinterleaver data segment 462 in shared memory syntax 416. The deinterleaved **data is subsequently processed by decoder** 423. The decoded data is stored in a decoded data segment 464 in shared memory syntax 416. The decoded data is then check for errors by CRC checker 424 and placed in a received user data segment 472. The received user data can then be extracted by an external entity via the

data/control interface syntax 426 on the external bus 490.

L Number	Hits	Search Text	DB	Time stamp
1	2330	mode adj2 table$1	USPAT; US-PGPUB	2002/09/15 11:04
4	2	(power adj2 save) with (mode adj2 table$1)	USPAT; US-PGPUB	2002/09/15 11:05
7	460	mode adj2 table$1	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:04
12	1	(power adj2 save) with (mode adj2 table$1)	EPO; JPO; DERWENT; IBM_TDB	2002/09/15 11:05

US-PAT-NO: 4485456
DOCUMENT-IDENTIFIER: US 4485456 A

TITLE: Data processor with R/W memory write inhibit signal

DATE-ISSUED: November 27, 1984

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Toyoda; Shinjiro	Yokohama	N/A	N/A	JP

US-CL-CURRENT: 711/152; 711/161 ; 713/340

ABSTRACT:

   A main power source voltage is compared with a reference voltage, when the
main power voltage drops lower than the reference voltage, an operation/halt
signal is formed, a read/write memory write inhibit signal is formed in
response to the operation/halt signal, and the read/write memory is inhibited
in operation. This write inhibit signal is formed by setting a D-type latch at
the timing of the transition of the NIF signal to active mode.

4 Claims, 14 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

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Detailed Description Text - DETX:

When the NIF signal to the AND circuit 47 becomes active (high) at the time t2,
the output RAME of the circuit 46 becomes high at this timing. Therefore, the
writing to the RAM 22 is inhibited. Since the OH signal is yet high as shown
in FIG. 6(c) at this time, the circuit 46 in FIG. 5 operates in the stand-by
RAM WRITE PROTECT mode as seen from the TABLE 1. Thereafter, the signal OH
becomes, as shown in FIG. 6(c), low, and then the CPU is operated in **POWER SAVE
mode as seen from the TABLE** 1. When the V.sub.DD is gradually recovered from
the time t3 in FIG. 6(a), the signals OH, WI sequentially become high, and
after the signal WI becomes high, the flag is cleared by the software. Then,
the RAM 22 will perform an ordinary operation as seen from the TABLE 1. In
this manner, the WRITE inhibition of the RAM 22 can be preferably performed by
the hardware even if the D-type latch is not used.

US-PAT-NO: 5691948
DOCUMENT-IDENTIFIER: US 5691948 A

TITLE: Memory apparatus

DATE-ISSUED: November 25, 1997

INVENTOR-INFORMATION:
NAME	CITY	STATE	ZIP CODE	COUNTRY
Sakabe; Tetsuya	Higashine	N/A	N/A	JP

US-CL-CURRENT: 365/227; 365/226 ; 713/324 ; 713/330

ABSTRACT:

    A measuring unit measures a time (T) of a command interval by setting the
end of a command generated from an upper apparatus to a start timing or by
setting the start of the reception of the next command to a stop timing. A
timing deciding unit varies a plurality of timings to perform a power saving on
the basis of the measurement time of the command interval which was measured by
the measuring unit. A power save control unit controls the apparatus to a
power saving mode for a time interval from the timing decided by the timing
deciding after the end of the execution of the command received from said upper
apparatus until a timing when a next command is obtained.

18 Claims, 19 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 14

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Detailed Description Text - DETX:

FIG. 11 shows an embodiment of the mode table in FIG. 10. First, threshold
times T1, T2, and T3 are determined as table addresses for the measurement time
(T). In the mode 1, a time zone less than T1 is set as an address. In the
mode 2, a time zone which is equal to or larger than T1 and is less than T2 is
set as an address. In the mode 3, a time zone which is equal to or larger than
T2 or is less than T3 is set as an address. In the mode 4, a time zone which
is equal to or larger than T3 is set as an address. In correspondence to the
mode numbers 1 to 4 according to an increase in measurement time (T) of the
command interval, the disk apparatus in FIG. 1 is divided into four circuit
units of the R/W circuit unit, clock generating circuit, VCM driver, and
SPM/cooling fan as power save control information and are set to the circuit
units as targets of the power saving. The disk apparatus is divided into the
circuit units by a method similar to that in case of the first invention of
FIG. 2. The **power save** control information in the **mode table** of FIG. 11, with
regard to the mode numbers 1 to 4, a mark "o" in the corresponding frame
denotes that the circuit unit shown by the mark "o" becomes the target circuit
unit of the power saving in the relevant mode. The circuit units as targets of
the power saving are determined so that the number of circuit units as targets
of the power saving increases with an increase in the command time interval
(T). In response to the increase in measurement time (T) of the command
interval, the number of circuit units as targets of the power saving is
increased in accordance with the order of the circuit units of short return

times which are required until the circuit units enter the normal operating
states after the power-on. That is, the return time of the R/W circuit unit at
the time of the power-on is on the order of microseconds and the R/W circuit
unit can be instantaneously returned to the operating state. In case of the
clock generating circuit 38, since the frequency dividing ratio is changed in
the power saving mode and the clock period is increased, the clock generating
circuit 38 can be also returned to the original operating state in the return
time on the order of microseconds. On the other hand, in case of the driver 48
of the VCM 50, in order to recover the servo control of the VCM 50 from the
power shut-off state to the normal operating state, for example, a return time
of about 100 to 200 msec is needed. Further, with respect to the driver 54 and
spindle motor 56, a relatively long return time of, for example, about 3
seconds is needed until the disk medium reaches a predetermined rotational
speed by the power-on. With regard to the cooling fan motor 60, the return
time at the time of the power-on does not particularly cause a problem.

Detailed Description Text - DETX:

Referring again to FIG. 10, subsequent to the **mode table** 166, the **power save**
control unit 68 is provided. The **power save** control information in FIG. 11 in
any one of the modes 1 to 4 selected with reference to the **mode table** 166 by
the measurement time (T) of the measuring unit 62 is set into the **power save**
control unit 68. In the set state of the power save control information, the
power save control unit 68 monitors the end of the execution of the command
received. When the execution of the command is finished, the power save
control according to the power control information which was set at that time
is performed. Specifically speaking, the power save control line shown by a
broken line is connected from the MPU 36 to the circuit unit as a target of the
power saving in the disk controller 12 in FIG. 1. The power save control line
sets and resets the bit data for the register to control the power saving of
each circuit unit. For example, in the power save control unit 68 in FIG. 10,
in correspondence to the contents of the power save control in FIG. 11, the bit
data is set and reset for the register 70 for reading and writing, register 72
for the clock generating circuit, register 74 for the VCM, and register 76 for
the SPM. In the embodiment of the circuit for performing the power saving by
the shut-off of the power supply by the power save control unit 68, the circuit
of FIG. 5 shown as a general form is used. The circuit of FIG. 6 is used as a
circuit for the power saving in the clock generating circuit 38 in FIG. 1.

Detailed Description Text - DETX:

A flowchart of FIG. 12 shows the measuring process by the measuring unit 62 in
FIG. 10. The processing steps in the flowchart are similar to those in the
first invention of FIG. 7 except the decision of the power saving mode in step
S10 and the setting of the power saving mode in step S11. The deciding process
of the power saving mode in step S10 is executed in the case where the
difference between the measurement times is equal to or larger than the
predetermined value in step S9. With reference to the **mode table** 166, for
example, the **power save** control information of the mode number corresponding to
the current command time interval (T) is selected from the table contents of
FIG. 11. The selected power save control information is set into the power
save control unit 68 in step S11. In step S12, the current measurement value
(T) is set into the EEPROM 42 and is updated.

Detailed Description Text - DETX:

FIG. 13 shows a power saving mode deciding process in step S10 in FIG. 12 as a
subroutine. The subroutine relates to the table contents of FIG. 11 as a
target. First in step S101, the measurement value (T) is read. In step S102,
a check is made to see if the measurement value (T) is less than (T1=5 sec).
When (T) is less than (T1=5 sec), the power save control information in the

mode 1 is selected in step S105. In step S102, when (T) is not less than (T1=5 sec), a check is made in step S103 to see if (T) is equal to or larger than (T1=5 sec) and is less than (T2=30 sec). When (T) lies within the above range, the power save control information in the mode 2 is selected in step S106. When (T) is out of the range in step S103, step S104 follows and a check is made to see if (T) is equal to or larger than (T2=30 sec) and is less than (T3=60 sec). When (T) lies within this range, the power save control information in the mode 3 in step S107 is selected. When (T) is out of the range in step S104, (T) is equal to or larger than (T3=60 sec), so that step S108 follows and the power save control information in the mode 4 is selected. In the selection of the **power save** control information based on the measured command time interval (T), it can be selected with reference to the **mode table** 166 prepared in the RAM or the like as shown in the functional block diagram of FIG. 10 or can be also selected by the execution of the value described on the program as shown in the subroutine of FIG. 13.

Detailed Description Text - DETX:

A flowchart of FIG. 14 relates to the processes of the power save control unit 68 in FIG. 10. First in step S1, a check is made to see if the command from the upper apparatus has been received. When the command is received, step S2 follows and the command is interpreted and executed. In step S3, a check is made to see if the execution of the command has been finished. When the end of the execution is discriminated, step S4 follows and with reference to the **mode table** 166 based on the measurement time (T) at that time, the power saving process according to the **power save** control information which has already been set is executed. That is, data bit 1 is set into the registers of the circuit units designated by the power save control information, thereby shutting off the power supply. Among the designated circuit units, with respect to the clock generating circuit 38, the clock frequency is reduced by switching the frequency dividing clock and the operating speed of the MPU 36 is decreased, thereby reducing the current consumption. In step S5, a check is made to see if the command from the upper apparatus has been received during the power saving. When the command is received, step S6 follows and the power saving mode is reset, namely, data bit 0 is set into the register of each circuit unit, thereby restarting the power supply and recovering the clock frequency. In step S7, a check is made to see if the set-up in association with the power save reset has been completed. When the completion of the set-up is confirmed, step S2 follows, the command received in the power saving state is analyzed and the corresponding process is executed.